

60 GHZ FRONT-END COMPONENTS FOR BROADBAND WIRELESS COMMUNICATION IN 130 NM CMOS TECHNOLOGY

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Abstract. The over 5 GHz available spectral space allocated worldwide around the 60 GHz band, is very promising for very high data rate wireless short-range communications. In this article we present two key components for the 60 GHz front-end of a transceiver, in 130 nm RF CMOS technology: a single-balanced mixer with high Conversion Gain (CG), reduced Noise Figure (NF) and low power consumption, and an LC cross-coupled Voltage Controlled Oscillator (VCO) with very good linearity, with respect to V_{ctrl} , and very low Phase Noise (PN). In both circuits, custom designed inductors and a balun structure for the mixer are employed, in order to enhance their performance. The VCO's inductor achieves an inductance of 198 pH and a quality factor (Q) of 30, at 30 GHz. The balun shows less than 1° Phase Imbalance (PI) and less than 0.2 dB Amplitude Imbalance (AI), from 57 to 66 GHz. The mixer shows a CG greater than 15 dB and a NF lower than 12 dB. In addition, the VCO achieves a Phase Noise lower than -106 dBc/Hz

at 1 MHz offset, and shows great linearity for the entire band. Both circuits are biased with a 1.2 V supply voltage and the total power consumption is about 10.6 mW for the mixer and 10.92 mW for the VCO.

Key words. 60 GHz Band, Millimeter-Wave Frequency, Down-Conversion Mixer, Integrated Balun, VCO, Cross-Coupled, Coplanar Waveguide (CPW), RF CMOS Technology

1 Introduction

The increasing demand for high data rate wireless communication in the last few years, has drawn a large commercial interest for the Millimeter-Wave (MMW) technology and more specifically for the unlicensed 57 to 66 GHz band. The wide allocated spectrum around 60 GHz is the main reason, which can be used for the implementation of all kinds of short-range (<1 km) wireless communication systems. In addition to the provided extensive bandwidth for future wireless personal and local area networks (WPAN,WLAN), adoption of wireless connectivity will soon be necessary, due to the

massive amount of the deployed portable devices (Smart-phones, tablets etc.). In addition, the millimeter-wave front-end transceiver technology is growing rapidly. The available spectrum ranges from 5 to 9 GHz depending the country, and has four sub-channels of approximately 2.16 GHz wide, as shown in Fig. 1. The possible applications which benefit from this extremely wide available spectrum in the 60 GHz band around the world, are many: (a) Wireless Personal and Local Area Networks (WPAN/WLAN) [1], (b) replacement of the wired connection between High-Definition devices (HDMI cable) from point-to-point streaming video links at 60 GHz [2], (c) Wireless ad-hoc communications e.g. notebook to notebook, notebook to printer, notebook to camera, camera to printer, notebook to TV, tablet to camera, camera to TV etc., (d) Wireless Sensor Networks (WSN) and many other applications.

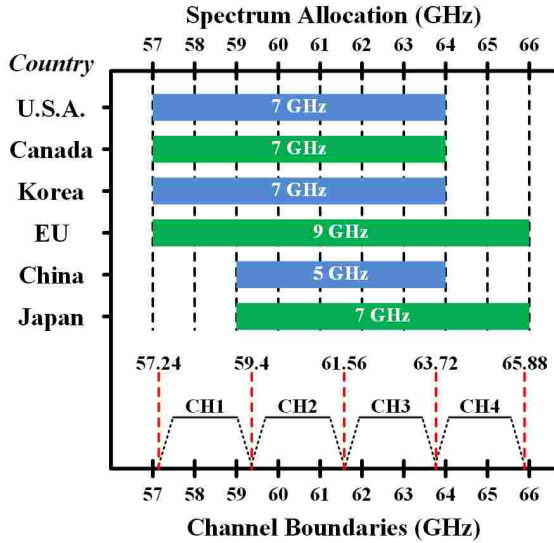


Fig. 1: Available spectrum around the 60 GHz band in different countries

For all these applications, key components of the receiver's system are the down-conversion mixer and the VCO for both homodyne and heterodyne wireless transceivers architectures. Fig. 2 depicts a general receiver architecture. The VCO and the mixer have a very

important purpose: the VCO, as a key component of the frequency synthesized LO, has to provide the appropriate signal in order to be used by the down-conversion mixer for converting the high-frequency input RF signal to a lower intermediate frequency suitable for further processing. The mixer has to provide high Conversion Gain (CG), low Noise Figure (NF) and wide bandwidth. The CG needs to be high enough in order to compensate for the noise contribution of the following stages in a receiver architecture. Additional critical parameters in a mixer design, are the linearity parameters: 1dB Compression Point (CP1dB) and 3rd-order Input Intercept Point (IIP3). In recent literature [4]-[7], have been proposed several implementations of down-conversion mixers for 60 GHz applications. In all these implementations, there is a lack of variability concerning the critical characteristics of a down-conversion mixer: bandwidth, CG, NF, linearity and power consumption. As far as the VCO is concerned, low phase noise (PN), high linearity considering the tuning control voltage and broadband operation are the most critical parameters. The VCO has to achieve low phase noise (PN) for entire range of the frequency bands while maintaining low power consumption.

In this article, are presented the designed circuits and the results from simulation of a single-balanced mixer with high and fully controllable CG, low NF and low power consumption, and a cross-coupled LC Voltage Controlled Oscillator (VCO) at 30 GHz with linear performance and very low PN. The proposed single-balanced mixer provides the capability of controlling the CG and simultaneously the available bandwidth using an alternative design of the current bleeding/injection technique presented in [5]. On the other hand, the VCO using a shielded Coplanar Waveguide Inductor (CPW) provides low PN and low power dissipation covering a wide bandwidth. The careful design and optimization through thorough Electromagnetic (EM) Simulations, of the passive devices (Inductors, Baluns etc.) was very critical for both circuits. The per-

formance of both components makes them very promising for 60 GHz applications.

The design of the proposed mixer topology is presented in Section 2, along with the simulation results. In Section 3, the design of the Voltage Control Oscillator is demonstrated along with the results from simulation. In both cases, comparison results are provided with similar topologies found in literature.

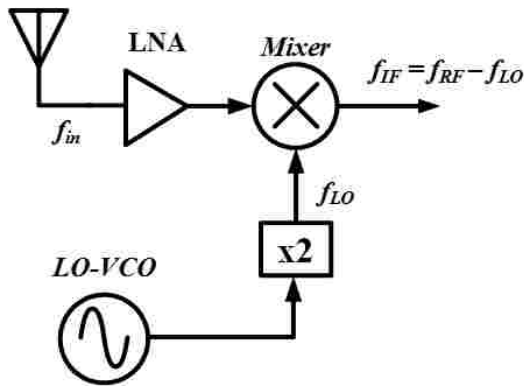


Fig. 2: Typical receiver architecture

2 Mixer Circuit Design and Simulation

A. Proposed Single-Balanced Mixer Circuit

The mixer topology consists of a typical single-balanced mixer, Fig. 3(a). In a single-balanced mixer the transistor M_1 , usually referred to as the RF transistor, forms the transconductor stage (g_m -stage) which is the main conversion gain contributor. The switching stage comprises from transistors M_2 - M_3 . Considering that we use a large LO signal, transistors M_2 - M_3 act as differential current switches and steer the RF current into one of the branches of the differential pair. In order to overcome the voltage headroom problem at the output node in the case of a resistive load, inductors L_1 and L_2 are used instead. The inductive load (L_1 and L_2) and the parasitic capacitances

of M_2 - M_3 form two resonating tanks at the desired IF frequency and results to higher CG. At such high frequencies the parasitic capacitance can significantly degrade the provided conversion gain and the resistive load can't counterbalance this effect [5]. Consequently, an inductive load is more suitable for millimeter wave applications. In the RF port the matching was achieved through a simple LC network along with the source degeneration inductor L_s . As for the LO port, the designed integrated balun significantly improved matching. In the proposed circuit a current source was used for biasing purposes along with the appropriate resistors (not shown in Fig. 3(a)) for settling the nodes to desired voltage.

In millimeter-wave applications, parasitic capacitances can significantly deteriorate the overall performance of the circuit. For the compensation of these parasitic capacitances (mainly the capacitances seen at source nodes of M_2 - M_3) we used an inter-stage inductor L_{peak} [4]. The compensation of these parasitic capacitances results to a substantial increase of the CG. A similar CG can be achieved by using a very large current for biasing. Besides the CG, the inter-stage peaking inductor improved also the NF, bandwidth and linearity of the designed mixer.

In addition, a very promising technique for further improving the performance of the mixer is the current bleeding technique [5]. In [5] simple resistors are used for implementing this technique but it doesn't give us any controllability of the flowing current. In our case, the PMOS transistor M_4 controls the current flowing through the switching stage by adjusting the value of the control voltage V_{BL} , Fig. 3(b). The different currents flowing through RF input g_m -stage and the LO switching stage have as result an increased CG and a significant noise reduction. Through the g_m -stage can flow a large current for higher CG and improved linearity but for the LO switching stage the current flowing has to be small for instantaneous switching and less noise contribution from

this stage.

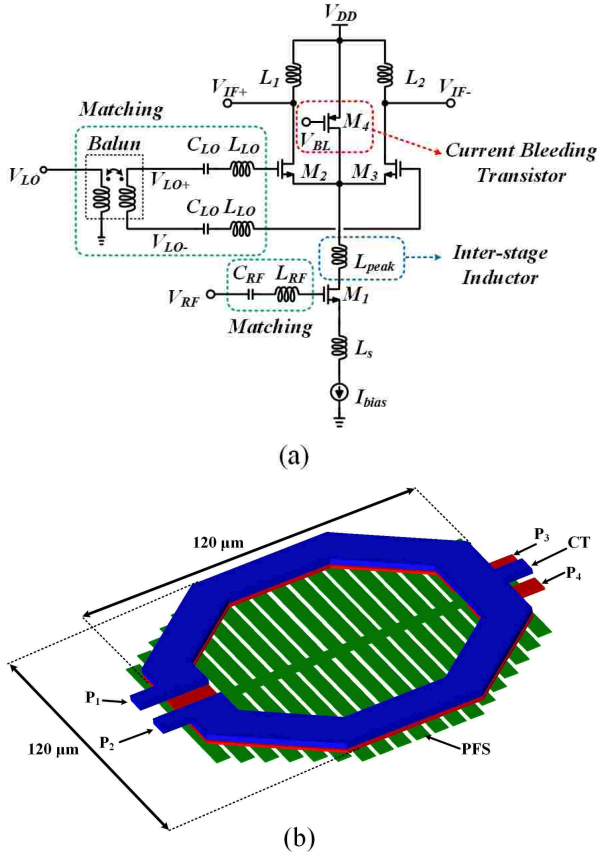


Fig. 3: (a) Designed single-balanced mixer and (b) integrated balun structure

B. Stacked Transformer-type Balun & EM Simulation Results

In Fig. 3(b) the layout of the designed integrated transformer type balun is demonstrated. Considering that a differential fast switching signal is needed for the LO stage of the single-balanced mixer, a passive transformer-type balun was designed. The use of a passive balun instead of an active one is mandatory at millimeter-wave frequencies. The balun structure has relatively small dimensions, $120 \times 120 \mu m^2$, and was designed using the

higher and thicker metal layers of the technology for lower losses. For a better isolation of the structure from the substrate and a significant improvement of the overall performance a Patterned Floating Shield (PFS) was designed using a lower metal layer [11]-[12]. Through extensive Electromagnetic Simulations (EM) by using the ADS Momentum, we obtained the optimum design considering the metal width, the number of turns and sizing in order to achieve low insertion loss, minimum phase and amplitude imbalances. It is reasonable for the signals at the differential output of the balun structure to show some imbalance in amplitude and phase considering the imperfections of the designed balun structure such as symmetry, and also the technology's characteristics. In order to quantify these imbalances (Amplitude and Phase Imbalances, AI and PI), the S-parameters are used through the following equations:

$$AI = 20 \times \log_{10} \left(\frac{|S_{21}|}{|S_{31}|} \right) \quad (1)$$

$$PI = \text{ang} \left(\frac{S_{21}}{S_{31}} \right) \quad (2)$$

Another significant parameter for characterizing the balun performance is Insertion Loss (IL). Considering that the balun structure is designed using metals, these metals suffer from conductor losses when high frequency signals pass through them. In addition, substrate losses due to the undesired currents formed at the substrate have a significant contribution to the overall IL. The signals at the differential output of the balun have exactly the half power of the input signal at an ideal balun. Although, in a non-ideal design such as our own, the IL is defined as the loss exceeding the power split loss. The stacked designed balun structure achieves an AI lower than 0.2 dB and a PI less than 1° through the entire 60 GHz band, Fig. 4. As for the insertion loss, it is maintained below 1.5 dB.

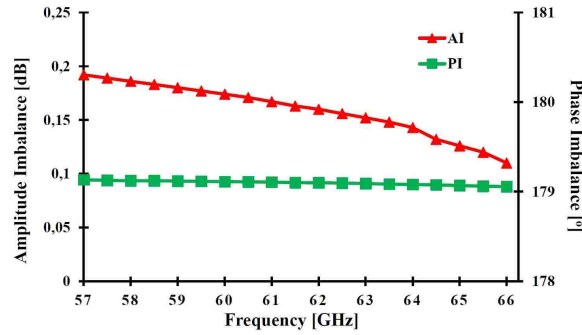


Fig. 4: AI and PI of the designed balun topology

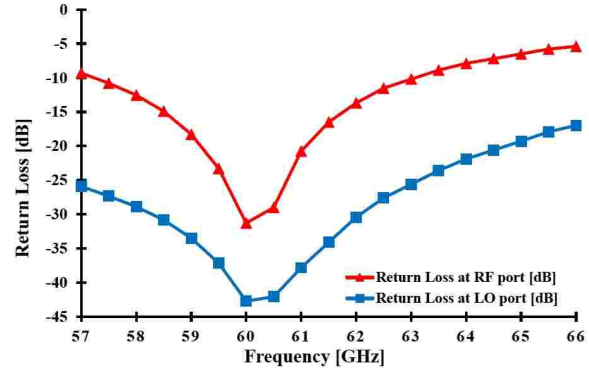


Fig. 5: RF and LO port return losses

C. Mixer Simulation Results

The proposed single-balanced mixer circuit is biased through a 1.2 V supply voltage and designed in a 130 nm CMOS technology using the Cadence software design environment. The design technology provides 8-metal layers in which the top two thick and ultra-thick metals are used for design of the custom inductors and the balun structure. In Fig. 5 are shown the S-parameter simulation results regarding the return losses at the RF and LO ports, verifying the achieved broadband matching for the entire band.

The RF signal was set at -30 dBm while the LO at 0 dBm, respectively, in order to obtain maximum CG and minimum NF. The frequency of the IF signal is selected to be 5 GHz considering a dual band, 5 and 60 GHz, transceiver front-end. The down-converted 5 GHz IF signal from the 60 GHz transceiver, can be processed by the same front-end components of the 5 GHz transceiver. In Fig. 6 and 7, the simulation results are presented for the CG and NF where the RF signal was set at 60.48 GHz and the LO at 55.48 GHz. These figures show

the difference in using the proposed design instead of a typical single-balanced mixer. The simulation results show that, the designed mixer circuit achieves a CG greater than 15 dB and a NF lower than 12 dB almost for the entire band around 60 GHz. The use of the peaking inductor and the modified current bleeding technique lead to a CG increase more than 9 dB and a NF suppression more than 8.5 dB, as shown in Fig. 6 and 7.

As mentioned above, the proposed single-balanced mixer exploiting the modified current bleeding technique can provide a conversion gain control by varying the V_{BL} voltage and controlling the current flowing through the switching stage. The provided gain control range is approximately around 6 dB while the V_{BL} voltage varies from 0 to 1 V. In Fig. 8 the variation of CG and NF versus the V_{BL} voltage is shown. In addition to the gain control, the -3 dB bandwidth is also varying from 2.4 GHz at the highest CG, to approximately 4 GHz at the lowest gain. The designed mixer topology showed a 1dB-Compression Point (CP1dB) of -10 dBm while the 3rd order Input Intercept Point (IIP3) is approximately about 1 dBm, considering the linearity parameters. Due to the high CG of the proposed mixer design, these linearity factors have low values. Although, deactivating the current-bleeding transistor, by adjusting the V_{BL} voltage value, we obtain a CP1dB of about -3.04 dBm

and an IIP3 around 7.2 dBm.

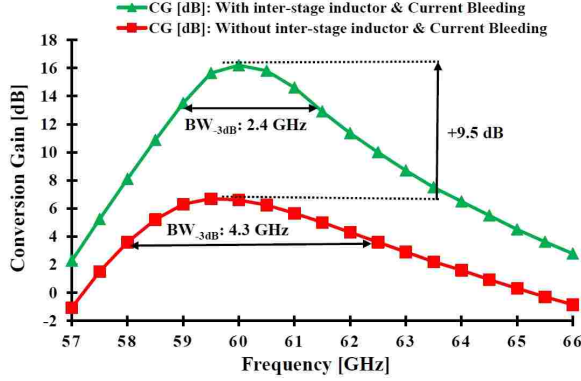


Fig. 6: CG vs RF frequency: with and without the peaking inductor & current bleeding

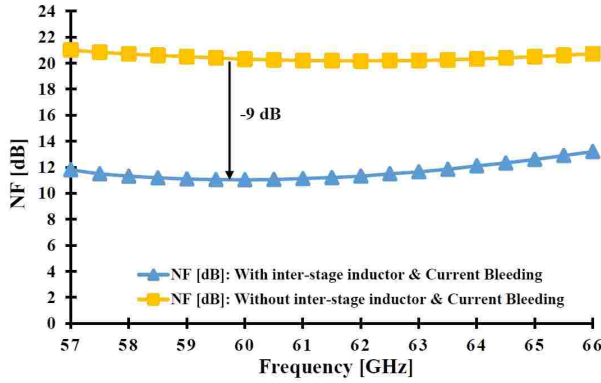


Fig. 7: NF vs RF frequency: with and without the peaking inductor & current bleeding

As was shown in Fig. 6, the achieved bandwidth (BW)

of the mixer is around 2.4 GHz and covers the channel specifications. The overall band coverage can be achieved by LO tuning as shown in Fig. 9. In order to cover the entire band, we selected four LO frequencies of 53.32 GHz, 55.48 GHz, 57.64 GHz and 59.8 GHz where the corresponding RF input frequencies for the four channels are: 58.33 GHz, 60.48 GHz, 62.64 GHz and 64.8 GHz, considering a 5 GHz down-converted IF signal. In Fig. 9

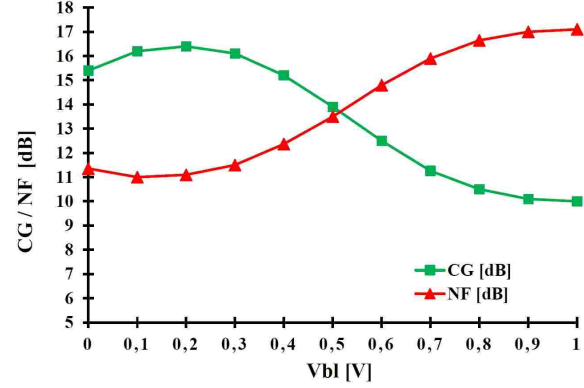


Fig. 8: CG & NF versus V_{BL} voltage

the CG and the NF of each channel by setting the above frequencies are presented. It is evident from Fig. 9 that, the proposed mixer retains almost constant CG and NF for the entire band.

In order to evaluate the performance of the proposed single-balanced mixer, the simulation results are compared with the results of similar state-of-art mixer topologies in recent literature [6]-[7], in Table I. It is evident from Table I, that with the proposed design we achieve much higher CG from the proposed mixer in [6], while the NF retains an approximately similar value. The ability to control the basic performance parameters of the proposed design, offers a more adaptable circuit and for example, by deactivating the current bleeding we obtain an improved 1-dB Compression Point (CP1dB) and 3rd order Input Intercept Point (IIP3). A critical parameter in a mixer design is power consumption, and the proposed mixer consumes approximately 6 mW less power than the one proposed in [6].

3 LC Cross Coupled Voltage Controlled Oscillator

A. Proposed VCO topology

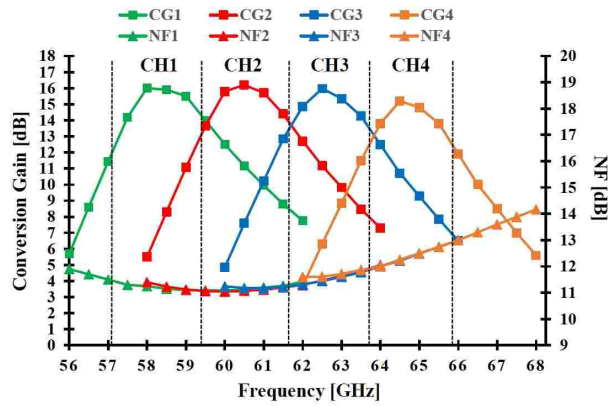


Fig. 9: CG and NF for the four channels of the 60 GHz band

TABLE I. SUMMARY AND COMPARISON OF MILLIMETER-WAVE MIXERS AT 60 GHz

Main Parameters	Reference		
	[6]	[7]	This Work
Topology	Single-Balanced	Single-Gate Mixer	Single-Balanced
Frequency [GHz]	54-65	57-64	57-66
Conversion Gain [dB]	9.1	> -2	>15
NF [dB]	12	-	<12
CP1dB [dBm]	-5	-3.5	-3.04*
IIP3 [dBm]	-	-	7.2*
Power Consumption [mW]	16.8	2.4	10.6
Technology	65 nm CMOS	130 nm CMOS	65 nm CMOS

*When current bleeding is deactivated.

Voltage controlled oscillators (VCO) are the most critical components of PLL-based local oscillators, because amongst the other components, VCOs have the main contribution to the phase noise (PN) of the entire system. This is why the performance of the VCO is a matter of major concern during the system design of a PLL. The VCO described in this paper is an integrated VCO designed in 130 nm technology with operating frequency of 28.46-33.62 GHz. In order to obtain simultaneously low PN and low power consumption over a wide bandwidth of operation, passive components with low losses are required. For this purpose, a Coplanar Waveguide (CPW) inductor has been designed.

The design is based on the topology of an LC cross-coupled oscillator, achieving a bandwidth of about 5

GHz. The PN is maintained under -100 dBc/Hz at 1 MHz away from the carrier and consumes approximately 10.92 mW. The resulting negative- g_m (LC cross-coupled) topology has been chosen for this design because of its simplicity, the circuit's robustness and the resulting low phase noise. An insightful approach to describe such an oscillator, is to consider it as a combination of a parallel LC tank and an active network, which serves as a negative resistance for the compensation of the energy loss in the tank.

Although modeling and evaluation of a VCO's phase noise is a very complex and challenging issue, Leeson's equation can be used for a rough estimation of the oscillator's single-side band phase noise spectrum. The main contributors and the main factors that play significant role in oscillator's phase noise are also described in (3) below:

$$L(f_m) = 10 \times \log_{10} \left\{ \frac{1}{2} \times \left[\left(\frac{f_0}{2 \times Q_l \times f_m} \right)^2 + 1 \right] \times \right. \\ \left. \times \left(\frac{f_c}{f_m} \right) \left(\frac{FkT}{P_s} \right) \right\} \quad (3)$$

In Eq. (3), f_0 is the carrier frequency, Q_l is the loaded quality factor (Q), f_m is the offset from the carrier frequency, f_c is the 1/f corner frequency, F is the noise factor of the amplification process, P_s is the Oscillator's output power, k is Boltzmann's constant and T is the absolute temperature in Kelvin.

Most of the factors which are presented in Leeson's equation express natural constants and the frequency of operation, and therefore, are not affected by circuit design. On the other hand, quantities like noise factor, output power and loaded Q are parameters that depend on the design of the oscillator and on the technology process used for the design of the oscillator. Especially loaded Q is a parameter of major concern, because it heavily affects the VCO's phase noise and at the same time, depends on both electrical and physical design.

One of the most critical components, considering the quality factor, is the inductor. However, it is very difficult to design a conventional inductor with low losses and high quality factor (Q) at the frequency of 30 GHz. For this design a CPW has been designed in order to obtain a high Q inductor. In Fig. 10, the layout of this inductor is presented. For the implementation of the CPW, the top metal of the technology has been chosen for obtaining the lowest possible losses. Under the inductor a Patterned Ground Shield (PGS) has been placed for the isolation of the inductor from the substrate's noise. The structure of the shield has been designed seven metal layers below top metal and has been optimized in order to reduce the effect of Eddy Currents. Thus, the structure of the CPW achieves an inductance of 198 pH and a quality factor of 30, at 30 GHz. More specifically in Fig. 11 and 12 the inductance (L) and the quality factor (Q) of the CPW are depicted, respectively. Firstly, it is shown that an inductance of 200 pH can be obtained using a relatively low area CPW inductor. The dimensions of the inductor are $193 \times 200 \mu\text{m}^2$. In addition this inductor has such a high Self-Resonant Frequency (SRF), which makes this structure suitable for oscillators operating in frequency of 30 GHz. Finally, the quality factor of the inductor is higher than 30 for the whole bandwidth of operation. The implementation of the CPW inductor has been based on Electromagnetic Simulations using Advanced Design System software.

In Fig. 13, the design of the proposed circuit is presented. The LC tank consists of the CPW inductor and a varactor, which is responsible for the frequency tuning. Nevertheless, the varactor cannot be used to cover the whole bandwidth of 5 GHz, because this choice would demand a very high gain of the VCO, which would result in degrading the phase noise. For this reason, a solution involving both discrete tuning using banks of capacitors (coarse tuning), and fine tuning with the varactor, is preferable. Following this approach, the bandwidth has been divided in sixteen

bands, with every band being controlled by a switch.

Equation (4) shows the dependence of loaded Q on the on-resistance (R_{on}) of the bank of capacitor's switches, focusing again on the phase noise. It is obvious that every switch plays significant role in the overall quality factor and it may lead to phase noise degradation.

$$\frac{1}{Q_{\text{total}}} = \frac{1}{Q_L} + \frac{1}{Q_{\text{Var}}} + \frac{1}{Q_{\text{BankCap}}} \quad (4)$$

where $Q_{\text{BankCap}} = 2 \times \pi \times f \times R_{\text{on}} \times C_u$ and C_u is the capacitance unit value of the bank. Every other capacitance value of the bank of capacitors, is a power-of-two multiple of this unit value C_u . This is an effective way to maintain matching between the circuit's components.

In this design, for overcoming the above mentioned impact of the switches on Q, four different banks of capacitors and their combinations, based on Boolean logic, have been used to implement the sixteen bands. As a result only four switches are used to control the sixteen frequency bands. Despite the fact that there are only four banks of capacitors, every one of them negatively affects the total quality factor and results in phase noise degradation. For this reason, variability in bias current is implemented by a combination of current switches.

As far as the design of the bands is concerned, they are implemented with the use of capacitors of $C = 14 \text{ pF}$. However, the technology doesn't offer capacitors suitable to implement the banks of capacitors. For this purpose, custom capacitors have been designed in order to meet the specifications of low capacitance and high quality factor. The implementation of the capacitors has been based on Electromagnetic Simulations using Advanced Design System software.

Moreover, the oscillator frequency changes with temperature and bias current variations. These changes are primarily due to the alteration in MOSFET's intrinsic capacitance. Even if the frequency bands are carefully

designed, often due to these changes in frequency, blind zones between the bands cannot be avoided. For this reason, in the proposed architecture a band overlap is chosen in order to ensure the undisrupted function of the VCO. As it's been mentioned above, phase noise highly depends on the gain of the VCO. This approach also offers the advantage that, due to the band overlap, it is possible to use for a specific frequency the band where the gain is lower, resulting in lower phase noise. **B.**

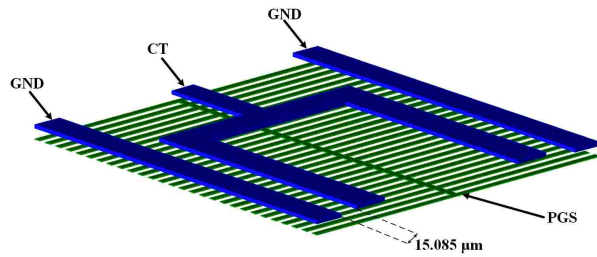


Fig. 10: Coplanar Waveguide Inductor (CPW Inductor)

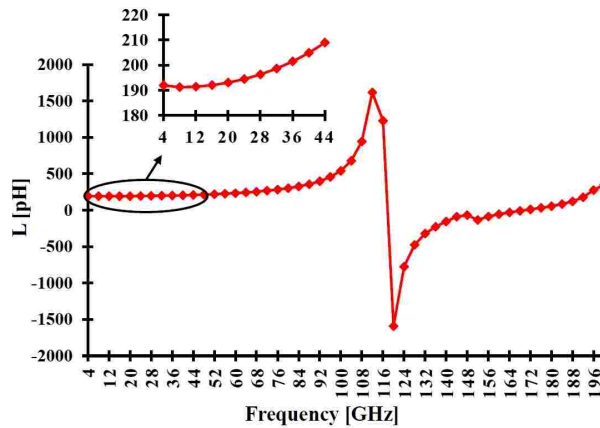


Fig. 11: Inductance versus frequency

Simulation Results

In Fig. 14 and Fig. 15, the simulations results are presented. Fig. 14 shows the frequency bands of operation, where bandwidth coverage and the overlap between the bands are depicted. The phase noise of every band is shown in Fig. 15. It must be noted, that the VCO shows

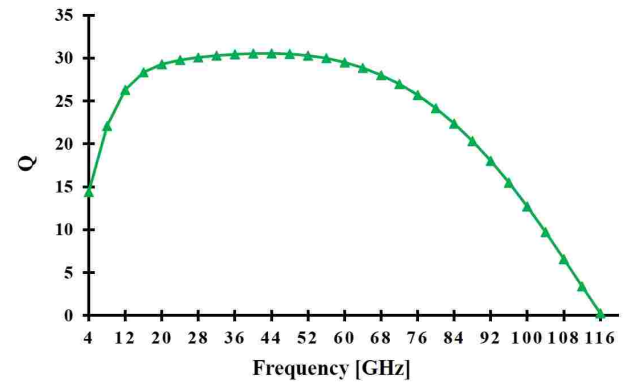


Fig. 12: Quality factor versus frequency

a phase noise under -100 dBc/Hz at 1 MHz away from carrier almost through the whole bandwidth of operation. In Table II, the overall performance parameters of the proposed VCO are summarized and compared with alternative promising topologies from the literature [8]-[9], at the same frequency band. The proposed VCO, achieves much lower phase noise with less power consumption.

4 Conclusion

Two very important components of a wireless receiver are presented in this article: a single-balanced mixer topology and a cross-coupled LC Voltage Controlled Oscillator (VCO). The proposed mixer design achieves a CG higher than 15 dB and a NF lower than 12 dB approximately, for the entire band around 60 GHz. Additionally, from the simulation results it can be seen that CP1dB and IIP3 are around -3.04 dBm and 7 dBm, respectively. The designed mixer circuit consumes power around 10.6 mW. On the other hand, the VCO shows a phase noise better than -105 dBc/Hz at 1 MHz offset, over a 5 GHz bandwidth with low power consumption at 30 GHz. Both of the components were designed in 130 nm CMOS technology.

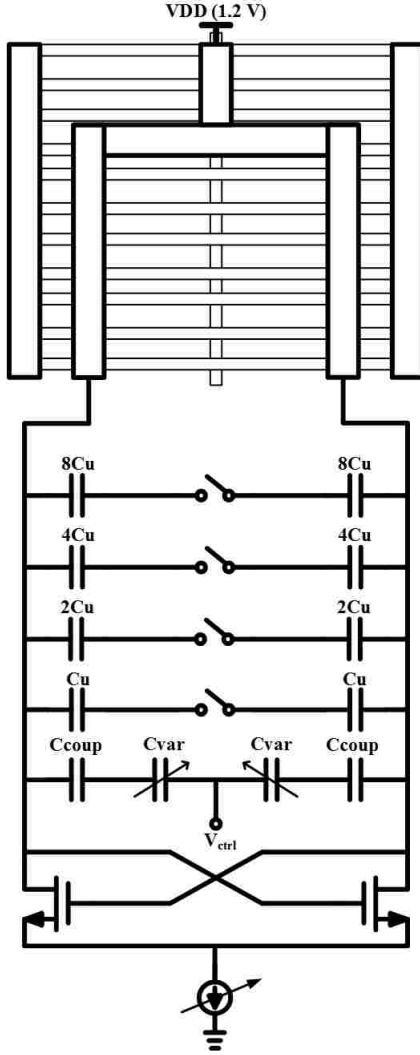


Fig. 13: LC Cross-Coupled VCO schematic

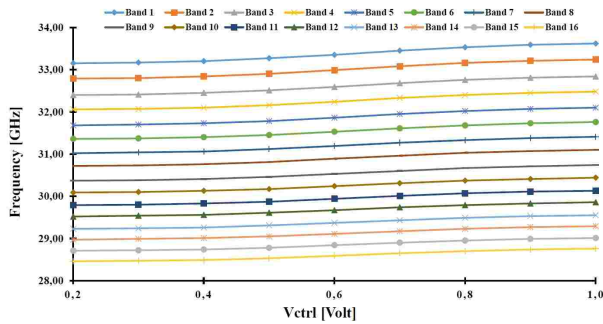


Fig. 14: Frequency Bands

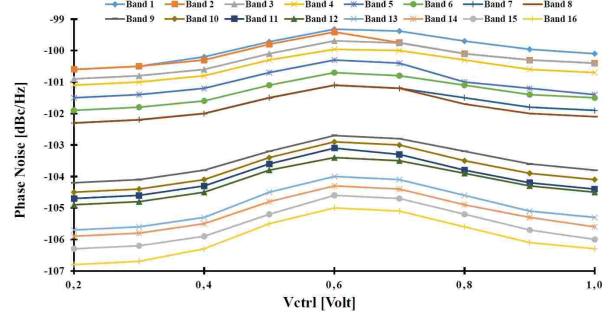


Fig. 15: Phase Noise in all bands

TABLE II. SUMMARY AND COMPARISON OF MILLIMETER-WAVE VCOs AT 30 GHz

Main Parameters	Reference		
	[8]	[9]	This Work*
Topology	Differential Colpitts	Differential LC Cross Coupled	Differential LC Cross Coupled
Frequency [GHz]	30.2-31	28.7-32.4	28.46-33.62
Phase Noise [dBc/Hz] @ 1MHz	-97.5	-104	-106.8
Power Supply [V]	2.8	1.2	1.2
Power Consumption [mW]	16.8	9	10.92
FoM*	174.7	184	186
Technology	0.35 μ m SiGe BiCMOS	90 nm CMOS	130 nm CMOS

*Based on simulation results. *FoM = $20\log_{10}(f_{osc}/f_m) - 10\log_{10}(P_{DC}[mW]) - PN(f_m)$, [8].

Acknowledgment

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